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Control of Ripple Eliminators to Improve the Power Quality of DC Systems and Reduce the Usage of Electrolytic Capacitors

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ABSTRACT The problem of voltage/current ripples has become a primary power quality issue for dc systems, which could seriously degrade the performance on both the source side and the load side and lead to reliability concerns. In this paper, a single-phase Pulse width modulation-controlled rectifier is taken as an example to investigate how active control strategies can improve the power quality of dc systems, reduce voltage ripples, and, at the same time, reduce the usage of electrolytic capacitors. The concept of ripple eliminators recently proposed in the literature is further developed, and the ratio of capacitance reduction is quantified. With such ripple eliminators, this power quality problem is formulated as a control problem to actively divert the ripple current on the dc bus. The main focus of this paper is to investigate how advanced control strategies could improve the performance of ripple eliminators. An advanced controller on the basis of the repetitive control is proposed for one possible implementation of ripple eliminators in the continuous current mode (CCM). Experimental results are presented to verify the effectiveness of the strategy with comparison to another ripple eliminator operated in the discontinuous current mode. It has been shown that the proposed instantaneous ripple-current diversion in CCM leads to a nearly fourfold improvement of performance.

INDEX TERMS Instantaneous diversion of ripple currents, CCM, DCM, ripple eliminators, voltage ripples, repetitive control, reliability, electrolytic capacitors.

I. INTRODUCTION

Proliferated renewable energy systems greatly promote the development of DC distributed power system, which enjoys flexible system configurations, high efficiency, and high density power delivery capability [2]. In such DC systems, ripple power is often not a major concern because a DC current is constant and there is not an issue of phase differences between voltages and currents. However, in many applications like hybrid electrical vehicles and wind power systems, rectifiers and inverters are commonly used and DC voltages are not ideal but have a significant amount of harmonic components [3]. Because of the harmonic components in the voltages and the resulting ripple currents, ripple power has become a major power quality issue in DC systems. For systems powered by photovoltaic panels, batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the lifetime and long-term reliability of photovoltaic panels, batteries and fuel cells [3]–[6]. During the charging mode of a battery, an external voltage with large ripples could lead to an immoderate chemical reaction. During the discharging mode, ripple currents drawn from a fuel cell can degrade the system efficiency significantly and even make it unstable [7]. Generally, current ripples should be maintained less than 10% of the rated current for batteries [8]. In order to reduce the ripple current and smooth the external voltage on batteries and fuel cells, bulky capacitors or ultracapacitors are often connected in parallel with them [9]. Large electrolytic capacitors are also often needed to level and smooth the DC-bus voltage of inverters and rectifiers [10]. For volume-critical and/or weight-critical applications, such as electrical vehicles [8] and aircraft power systems [10], the volume and weight of electrolytic capacitors could be a serious problem.

Because of limited lifetime of electrolytic capacitors, they are one of the most vulnerable components in power

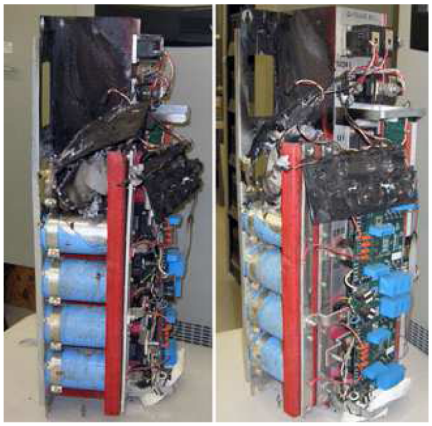

FIGURE 1. A damaged UPS inverter caused by the degradation of electrolytic capacitors. Source: http://blog.eecnet.com/eecnetcom/bid/27236/Why-Preventive-Data-Center-Maintenance-is-Important.

electronic systems [11], [12]. According to [13], more than half of faults of static converters are caused by degraded electrolytic capacitors. On the other hand, the presence of large voltage ripples is an essential factor that accelerates the degradation of electrolytic capacitors [11]. Figure 1 shows a damaged UPS inverter assembly, the damage was caused by the ageing electrolytic capacitors. This may cause a big disruption in critical loads, which in turn could lead to a huge cost. As a result, in order to enhance the reliability of power electronic systems, it is highly desirable to minimise the usage of electrolytic capacitors and it is very attractive if highly-reliable small capacitors like film capacitors could be used to achieve low-level voltage ripples. However, in applications involving bulky electrolytic capacitors, it is often inevitable to have a trade off between minimising the total capacitance required and suppressing voltage ripples. Another design degree of freedom, normally through active control, needs to be introduced to break this deadlock.

In principle, this power quality issue in DC systems stems from energy fluctuation, which can come from sources and/or loads of systems. Four main approaches have been developed in the literature to reduce or compensate energy fluctuation so that the voltage ripples can be reduced and the power quality in DC systems can be improved.

One approach is to inject harmonic currents to suppress the fluctuations of the input energy by changing the control strategy for the existing power switches in the system. In [14], it was proposed to inject third harmonic component to the input current so as to reduce the DC-bus capacitor in LED drivers. The analysis in these papers is based on the fact that decreased pulsating input power leads to decreased ripple power and capacitor volume on the DC bus, which can be achieved by controlling the input current. In [15], a similar concept was also adopted by distorting the input current to reduce the output capacitor. The essence of injecting harmonic currents or distorting the input current is to obtain a varied duty cycle to control the power switches, which changes the amount of energy delivered to the load in each fundamental cycle. This approach benefits with no added power components but the disadvantage of this approach is the increased total harmonic distortion (THD) of the input current.

The second approach is to use buck/boost DC/DC converters to construct two DC voltages across two capacitors that are connected in opposite polarity [16]–[18]. The sum of pulsating energy stored in the two capacitors are nearly equal to the system pulsating energy and hence, the pulsated energy does not appear on the DC bus. Both the DC-bus voltage ripples and the required DC-bus capacitance can be reduced.

The third approach is to add an active energy storage circuit in parallel with the DC-bus capacitor to bypass the ripple currents originally flowing through the DC-bus capacitor [10], [11], [19], [20]. The strategy proposed in [19] is such an example, with a circuit consisting of one capacitor, one inductor and two power switches. It absorbs and releases the ripple energy, respectively, during its two different half cycles. Due to the particular operating modes adopted, the current is compensated in terms of averaged values, instead of instantaneous values, so the remaining voltage ripples are still large although considerably reduced.

The fourth approach is based on connecting an active compensator in series with the DC bus line [21], [22]. The compensator basically behaves as a voltage source to offset the voltage ripples. Due to the series operation, the voltage stress of the added compensator is reduced. However, the current stress of the compensator is increased because the ripple power for a certain load is fixed. Due to the series connection, lines between the DC sources and loads should be cut off so that the compensator can be connected. However, for some DC systems, this can be a problem because of the widely-distributed sources and/or loads. Note that only the DC voltage after the compensator becomes clean without noticeable low-frequency ripples but the DC voltage before the compensator still suffers from large low-frequency ripples.

Some of the aforementioned approaches are only effective in some specific DC systems while the others are applicable to different kinds of DC systems. For example, the method of injecting harmonics to mitigate pulsating power is specially designed for rectifier systems [23]. In DC systems, there might be different kinds of widely-distributed sources and loads and hence, it is hard to apply this method to all sources and/or loads. From this point of view, it becomes obvious that the last two approaches are more effective to improve the power quality for general DC systems, although more power components are required. Compared to the fourth approach, i.e. adding a series eliminator, the third approach, i.e., adding a shunt eliminator, is more suitable for general DC systems because it does not need to cut off any lines for connecting eliminators. Shunt eliminators can be simply hooked onto the DC bus for the purpose of reducing voltage ripples to improve power quality in DC systems.

The main focus of this paper is to investigate how advanced control strategies could improve the performance of shunt ripple eliminators for DC systems, rather than optimizing the

system performance through topological design. It is found that the capability of diverting the ripple current away from the DC bus is the key for improving the performance. Hence, it is important to adopt a control strategy that is able to track periodic signals and the repetitive control strategy [24] is then applied to achieve instantaneous current tracking at a fixed switching frequency. Furthermore, it is preferred to operating the shunt ripple eliminator in the continuous current mode (CCM) rather than in the discontinuous current mode (DCM) because the current tracking is instantaneous in CCM but is in the average sense in DCM. Because the ripple current is diverted instantaneously in CCM, the voltage ripples can be reduced considerably. The boost topology in [25], where a flicker-free AC–DC LED driver with a flyback PFC converter was designed and the strategy, is taken as an example, because of its high efficiency compared to buck-type topologies [26], to demonstrate the performance improvement by designing a suitable controller. This topology was also investigated in the conference version [1] of this paper and also in [27] and [28]. It is a bidirectional boost converter that is able to divert the ripple current *instantaneously*. The voltage of the auxiliary capacitor is higher than the DC-bus voltage, which helps improve the efficiency performance [26], the current tracking performance and reduce the required capacitance to achieve the same performance. Compared to the conference version [1] of this paper, the new contributions of this paper include 1) analysing and revealing how active control strategies can help reduce voltage ripples and reduce total capacitance, which paves a way to design high performance controllers for different types of ripple eliminators; 2) quantifying the level of capacitance reduction, which is independent from applications and topologies; 3) optimizing the controller for ripple eliminators in which only one instead of two repetitive controllers are now required without affecting the system performance; 4) experimentally verifying the performance of the active control strategies.

The following parts of this paper are presented as follows. In Section II, a single-phase H-bridge Pulse width modulation (PWM) rectifier is taken as an example to analyse the ripple energy and ripple voltage in a DC system. In Section III, the concept of ripple eliminators is further developed and the level of reduction of capacitance is quantified. In Section IV, the operation principle of the ripple eliminator under investigation is discussed and in Section V the controller of the ripple eliminator is developed based on repetitive control. Experimental results with comparison to a ripple eliminator reported in the literature are provided in Section VI. At the end, conclusions are made in Section VII.

II. ANALYSIS OF RIPPLE ENERGY AND RIPPLE VOLTAGE

In order to facilitate the analysis in this paper, a single-phase H-bridge PWM-controlled rectifier as shown in Figure 2 is used as an example, with all the components assumed to be ideal to simplify the analysis in the sequel. Most of the findings can be easily applied to other applications.

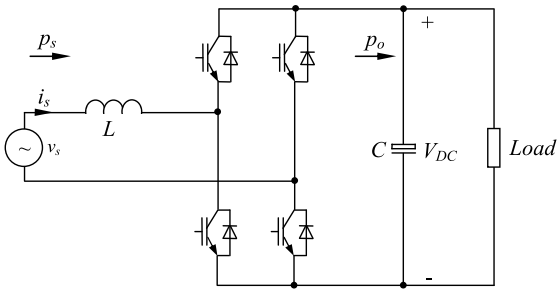

FIGURE 2. Single-phase H-bridge PWM-controlled rectifier.

If the input current of the rectifier is regulated to be sinusoidal as $i_s = \sqrt{2}I_s \sin(\omega t)$ and in phase with the input voltage $v_s = \sqrt{2}V_s \sin(\omega t)$, then the input power is

$$p_s = v_s i_s = V_s I_s - V_s I_s \cos(2\omega t), \tag{1}$$

where V_s and I_s are the RMS values of the input voltage and current, respectively, and ω is the angular line frequency. Note that the power drawn from the AC source consists of a constant $V_s I_s$ and a second-order ripple component $-V_s I_s \cos(2\omega t)$.

In order to analyse the voltage ripples of the DC bus, the net change of the energy stored in the DC-bus capacitor over a charging period (i.e. a quarter cycle of the supply), called the ripple energy, can be calculated as [10]

$$E_r = \frac{V_s I_s}{\omega}. \tag{2}$$

As demonstrated in [10], the voltage ripple (peak-peak) on the capacitor C can be given as

$$\triangle V_{DC} \approx \frac{E_r}{C V_{DC0}} \tag{3}$$

where V_{DC0} is the average value of the voltage V_{DC}. It is clear that, when increasing the capacitor C, the DC-bus voltage ripple is decreased but this increases the weight, volume and cost of the system and decreases the reliability of the system, which should be avoided if possible.

III. RIPPLE ELIMINATORS AND THE LEVEL OF CAPACITANCE REDUCTION

In order to break the deadlock between minimising the required capacitors and reducing voltage ripples, another design degree of freedom, called the ripple eliminator [19], can be introduced to replace the bulky DC-bus capacitor, as shown in Figure 3. The basic idea is to introduce an auxiliary capacitor C_a in the ripple eliminator so that the ripples on the DC bus can be transferred onto C_a. The voltage V_a across the auxiliary capacitor C_a is allowed to vary within a wide range with a large ripple $\triangle V_a$. This concept can be regarded as the general form of the strategies proposed in the literature, (e.g., [10], [25]).

Since the ripple eliminator is operated to divert the ripple energy on the DC bus to the auxiliary capacitor, there is no need to use a large electrolytic capacitor on the DC bus and

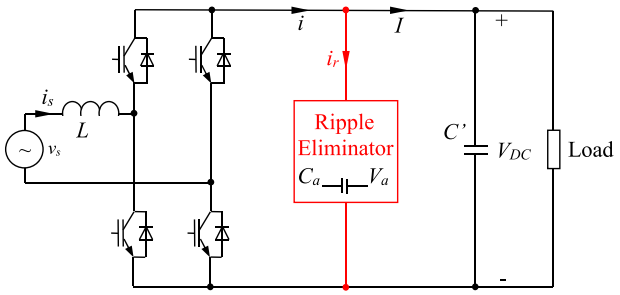

FIGURE 3. The concept of ripple eliminators.

the ripple energy on the auxiliary capacitor should be the same as the DC-bus ripple energy in the ideal case. Applying (3) to the auxiliary capacitor, there is

$$C_a \approx \frac{E_r}{\triangle V_a V_{a0}}, \tag{4}$$

where $\triangle V_a$ and V_{a0} are the peak-peak and average voltages of the auxiliary capacitor. Note that the ripple energy E_r is determined by the DC bus and not affected by the added ripple eliminator. Note also that the auxiliary capacitor is designed to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor is

$$r_a = \frac{\triangle V_a}{V_{a0}}. \tag{5}$$

Then (4) can be re-written as

$$C_a \approx \frac{E_r}{r_a V_{a0}^2}. \tag{6}$$

It is clear that for the same ripple ratio r_a, the capacitance is in inverse proportion to the square of the voltage across it, which means the auxiliary capacitance can be significantly reduced via increasing its operating voltage.

If the same ripple energy E_r needs to be taken care of by a DC-bus capacitor C, as shown in Figure 2, then, according to (3), the voltage ripple ratio r of the DC bus is about

$$r \approx \frac{E_r}{CV_{DC0}^2}. \tag{7}$$

This means the auxiliary capacitor needed can be reduced to

$$C_a \approx \frac{r}{r_a}(\frac{V_{DC0}}{V_{a0}})^2 C \tag{8}$$

by a factor of

$$R_d = \frac{r_a}{r}(\frac{V_{a0}}{V_{DC0}})^2 = \frac{\triangle V_a V_{a0}}{\triangle V_{DC} V_{DC0}}. \tag{9}$$

The capacitance C_a can be reduced by 1) allowing the voltage ripple ratio higher than that of the original DC bus, 2) adopting an operating voltage V_{a0} higher than V_{DC0} for C_a. The topology in [10] adopts a higher voltage ripple ratio and the strategy in [19] adopts both.

Here is a numerical example. If the auxiliary capacitor voltage is chosen four times of the DC-bus voltage then the maximum allowable ripple voltage ratio of the auxiliary capacitor is $r_a = 75\%$. Moreover, if the allowed ripple ratio of the original DC-bus voltage is $r = 5\%$, then the auxiliary capacitor can be reduced by a factor of $R_d = \frac{75\%}{5\%} \times 4^2 = 240$. Hence, it is not a problem to reduce the level of the total capacitance required by a factor of 100.

Note that (9) is independent of applications. It sets the basic guidelines for designing different ripple eliminators. Some other guidelines include: 1) a ripple eliminator needs to be able to provide bi-directional current path so that the ripple current can flow through; 2) the remaining level of DC-bus voltage ripples is determined by the performance of the ripple eliminator so the ripple eliminator needs to be controlled properly; 3) The hold-up time requirement [21], voltage stress and current stress should be considered to choose suitable capacitors. If the maximum voltage of the capacitor is determined, then increased capacitance means longer hold-up time and lower current stress, which are preferred in some applications [12]. As a result, there are several trade-offs that should be considered together when choosing the capacitors for certain applications. If all the ripple current in i is bypassed through the ripple eliminator then the DC-bus capacitor C' only needs to take care of the switching ripples and hence small capacitors can be used.

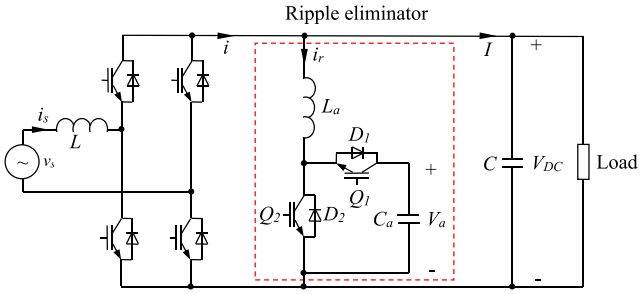

FIGURE 4. The ripple eliminator under investigation.

IV. THE RIPPLE ELIMINATOR UNDER INVESTIGATION

A. OPERATION PRINCIPLES OF THE RIPPLE ELIMINATOR

In this paper, a practical implementation of the ripple eliminator concept to be studied is shown in the dashed box of Figure 4, which is actually a bi-directional boost-buck converter. It can also be regarded as one phase of an inverter with the DC bus provided by the auxiliary capacitor C_a so it is able to divert a bidirectional current i_r away from the DC bus. This topology was studied in [25], where a flicker-free LED driver with a flyback PFC converter was designed and the strategy about how to remove the ripple energy through tracking the ripple current generated by the flyback converter was analysed in detail, and in [27] and [28], where an active filter for grid-tied PV applications was developed to reduce the low frequency current drawn from PV panels.

In order to track the ripple current, switches Q_1 and Q_2 can be controlled in two different switching modes. One is only to control Q_2 (Q_1, resp.) in the positive (negative, resp.)

half cycle of the ripple current, which corresponds to the charging (discharging) mode. In the charging mode, Q_2 is controlled by a PWM signal and Q_1 is always OFF, which provides the path for the positive half cycle of the ripple current i_r, and hence, the ripple eliminator is operated as a boost converter. In the discharging mode, Q_2 is always OFF and Q_1 is controlled by a PWM signal, which provides the path for the negative half cycle of the ripple current i_r, and the circuit is operated as a buck converter. Therefore, the direction of the current flowing through the auxiliary inductor can only be negative or positive in one switching period.

Another switching mode is to control the two switches complementarily. That means switches Q_1 and Q_2 are controlled by two inverse PWM signals to track the ripple current and the voltage across the auxiliary inductor can be V_{DC} and $V_{DC} - V_a$ depending on the ON-OFF combinations of these two switches. In one PWM period, if Q_1 is ON, Q_2 is controlled by an inverse signal to keep OFF and vice versa. Different from the previous operation mode, the inductor current can be positive or negative even during one switching period. This is a very good feature because the current can be tracked very well no matter at zero-crossing points or at large current ripple conditions. In the previous mode, the sharp turn at the zero-crossing points causes high harmonic content, which is hard for the controller to track. Since the final control objective is to reduce DC-bus voltage ripples, it does not matter if the auxiliary current ripple is slightly large because of the high switching frequency. With the same system parameters, large ripple means a small inductor is needed, which can reduce the size of the ripple eliminator. In this paper, in order to fully use the ripple eliminator under different working conditions, Q_1 and Q_2 are operated complementarily to track the ripple current.

B. SELECTION OF THE AUXILIARY INDUCTOR

Apart from the auxiliary capacitor C_a, there is another passive component, i.e., the auxiliary inductor L_a, that affects the performance of the ripple eliminator. In this subsection, how to select the L_a is discussed.

Here, the duty cycle and the PWM period time are denoted as d_r and T_r, respectively. As two switches Q_1 and Q_2 are operated complementarily, the ON time of Q_2 is $d_r T_r$ and the ON time of Q_1 is $(1 - d_r)T_r$ in one PWM period. Since the PWM frequency is much higher than the line frequency, it can be assumed that the current increased (to withstand the positive voltage V_{DC}) and decreased (to withstand the negative voltage $V_{DC} - V_a$) in these two modes are the same in the steady state. In other words, the current ripple $\triangle i_r$ is

$$\triangle i_r = \frac{V_{DC}}{L_a} d_r T_r = -\frac{V_{DC} - V_a}{L_a}(1 - d_r)T_r. \tag{10}$$

Therefore, the duty cycle d_r can be obtained as

$$d_r = 1 - \frac{V_{DC}}{V_a}. \tag{11}$$

The substitution of (11) into (10) leads to

$$\frac{L_a \triangle i_r}{V_{DC}} = (1 - \frac{V_{DC}}{V_a})T_r, \tag{12}$$

which can be re-written as

$$f_r L_a \triangle i_r = V_{DC}(1 - \frac{V_{DC}}{V_a}). \tag{13}$$

As expected, the product of the switching frequency f_r, the inductance L_a and the current ripple $\triangle i_r$ is a constant, which is determined by the DC-bus voltage and the auxiliary voltage. The auxiliary inductor current mainly includes the current ripple Δi_r and the ripple current to be injected into the DC-bus. Hence, the role of the DC-bus capacitor is to filter out this high frequency current ripple $\triangle i_r$, which could be achieved by a small capacitor.

In this case, the amplitude of the current ripple Δi_r is not a major concern. As long as the low frequency component of the inductor current is equal to the second-order harmonic current on the DC bus, the ripple voltage on the DC bus can be effectively eliminated. The high frequency part of i_r, which is Δi_r, can be large in order to reduce the inductance of L_a. However, a large Δi_r leads to a large current peak for the inductor and also aggravate the filtering burden of the capacitor C. Therefore, there is a trade off between L_a and $\triangle i_r$. In this work, in order to ensure the inductor is operated in the critical continuous current mode, the amplitude of $\triangle i_r$ is designed to satisfy

$$\Delta i_r \leq 2I_{rm}, \tag{14}$$

where I_{rm} is the peak value of i_r. Considering (12), the auxiliary inductance should be selected to satisfy

$$L_a \geq \frac{(1 - \frac{V_{DC}}{V_a})V_{DC}}{2I_{rm} f_r}. \tag{15}$$

On the other hand, the rising rate of the auxiliary inductor current should be greater than the maximum rising rate of the reference ripple current which appears at the zero-crossing point. If the reference ripple current is expressed as

$$i_r = I_{rm} \sin(2\omega t), \tag{16}$$

then the maximum rising rate of i_r can be obtained as

$$\frac{di_r}{dt} \mid_{t=0} = 2\omega I_{rm} = 4\pi f I_{rm}. \tag{17}$$

Accordingly, there exist

$$\frac{V_{DC}}{L_a} \geq 4\pi f I_{rm}, \tag{18}$$

and

$$\frac{V_a - V_{DC}}{L_a} \geq 4\pi f I_{rm}. \tag{19}$$

Combining the above two equations, then

$$L_a \leq \min\left(\frac{V_{DC}}{4\pi f I_{rm}}, \quad \frac{V_a - V_{DC}}{4\pi f I_{rm}}\right). \tag{20}$$

Combining it with (15), there is

$$\frac{(1-\frac{V_{DC}}{V_a})V_{DC}}{2I_{rm}f_r} \le L_a \le \min\left(\frac{V_{DC}}{4\pi f I_{rm}}, \quad \frac{V_a - V_{DC}}{4\pi f I_{rm}}\right), \tag{21}$$

i.e.,

$$1-\frac{1}{\frac{V_a}{V_{DC}}} \le \frac{2I_{rm}f_r L_a}{V_{DC}} \le \min\left(\frac{1}{2\pi}\cdot\frac{f_r}{f}, \quad \frac{\frac{V_a}{V_{DC}}-1}{2\pi}\cdot\frac{f_r}{f}\right), \tag{22}$$

where $I_{rm}f_r L_a$ reflects the voltage dropped on L_a caused by I_{rm} at the switching frequency f_r. This relationship is shown in Figure 5 and can be used to determine L_a. Note that L_a can be reduced via increasing f_r. Moreover, when I_{rm} is increased, L_a can be reduced.

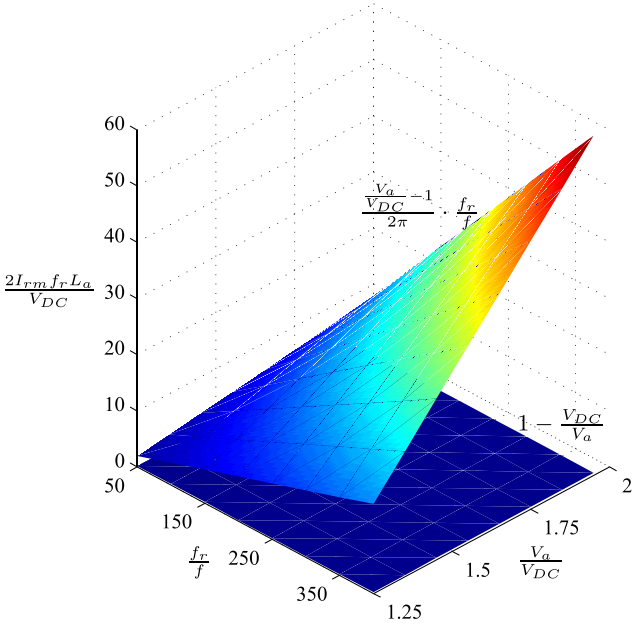

FIGURE 5. Selection of $\frac{2I_{rm}f_rL_a}{V_{DC}}$: between the two surfaces.

V. CONTROL OF THE RIPPLE ELIMINATOR

A. FORMULATION OF THE CONTROL PROBLEM

As discussed before, the DC voltage ripple is caused by the pulsating input energy. After the ripple eliminator is introduced to divert the ripple current from the capacitor C, the DC-bus voltage then becomes ripple free, apart from switching ripples, and equal to the DC-bus voltage. Hence, the current to be diverted should be

$$i_r = -\frac{V_s I_s}{V_{DC0}}\cos(2\omega t), \tag{23}$$

which is a second-order harmonic current. Note that the current i_r could be different for other DC systems but it does not affect the analysis above. The control objective of the ripple eliminator is then to instantaneously divert i_r in (23) away from the DC bus through the ripple eliminator so that the current flows through the load does not contain ripples other than switching ripples. In other words, the control problem is to instantaneously track the ripple current i_r that corresponds to the ripple power via controlling Q_1 and Q_2.

Tracking the i_r can be achieved in terms of either averaged values or instantaneous values, which corresponds to the DCM or CCM operation of the ripple eliminator. Of course, the current tracking performance in CCM is better than that in DCM. Hence, the CCM operation is preferred. On the other hand, the inductor will have a relatively large size in order to keep the ripple current continuous. This can be mitigated if the ripple eliminator can be operated at high switching frequencies. For example, if MOSFETs instead of IGBTs are used to construct the eliminator, then the switching frequency can be very high, e.g., at 200 kHz, so that only a small inductor is needed. When it is operated in DCM, the inductor can be smaller but the maximum current flowing through the switches is much higher in DCM than that in CCM because of the average tracking. High current means high cost for switches.

In this paper, the CCM operation is chosen because of its high performance for current tracking. The ripple current tracking can be achieved in two steps: 1) to generate a reference ripple current and 2) to track the reference ripple current. Moreover, in order to make sure that the current tracking can be achieved properly, the voltage across the auxiliary capacitor C_a should be regulated as well. The proposed overall control strategy is shown in Figure 6, which is explained in detail in the following subsections.

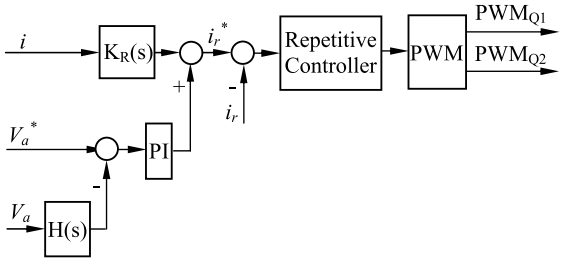

FIGURE 6. Control strategy for the ripple eliminator.

B. REGULATION OF THE AUXILIARY CAPACITOR VOLTAGE

The operation of the ripple eliminator relies on a properly regulated the voltage across the auxiliary capacitor, which is designed to allow a significant amount of ripples. For the purpose of maintaining the average DC component at a certain value, a low-pass filter can be adopted to remove ripples. Here, the following low-pass filter

$$H(s) = \frac{1-e^{-\tau s/2}}{\tau s/2}, \tag{24}$$

in which τ is chosen as the system fundamental period, is used to filter out other components so that the average value of the voltage can be extracted for control. Once the average voltage is obtained, it can be easily regulated at a given value V_a^* by

using a PI controller, as shown in Figure 6, via charging or discharging the ripple eliminator. It is also possible to design the controller to regulate the maximum or minimum value of the voltage, as reported in [19].

C. GENERATION OF THE REFERENCE RIPPLE CURRENT i_r^*

The second-order harmonic current of the current i between the rectifier and the ripple eliminator can be extracted by using the following resonant filter

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{25}$$

tuned at the second harmonic frequency with $\xi = 0.01$, $h = 2$, and $\omega = 2\pi f$. If the harmonic current has components at other frequencies, then $K_R(s)$ can be designed to include the corresponding term. For example, if there is a 3rd-order harmonic current, then $K_R(s)$ can include a term with $h = 3$. The extracted current can be added to the output of the PI controller that regulates the auxiliary capacitor voltage to form the reference ripple current i_r^*; see Figure 6.

D. DESIGN OF A CURRENT CONTROLLER TO TRACK THE SECOND-ORDER RIPPLE CURRENT

As explained before, the control problem is essentially a current tracking problem. Since the reference ripple current is periodic, the repetitive control strategy [29], [30] can be adopted to achieve excellent tracking performance with a fixed switching frequency, as shown in Figure 6.

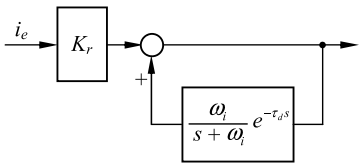

FIGURE 7. The repetitive controller.

A repetitive controller contains an internal model, which is a local positive feedback loop involving a delay term and a low-pass filter, as shown in Figure 7. It introduces high gains at the fundamental and all harmonic frequencies of interest and hence, it is able to eliminate periodic errors [31], according to the internal model principle [32]. From the controllers designed with advanced control algorithms, e.g., the ones in [30], the controllers that work with the repetitive control strategy can be very simple. In this paper, since the problem is a current tracking problem, the proportional controller K_r cascaded with the internal model obtained in [29] and [30] with the H_∞ control strategy, as shown in Figure 7, is adopted. Here, $i_e = i_r^* - i_r$ is the current tracking error.

Based on the analysis in [30] and [33], τ_d is selected as

$$\tau_d = \frac{\tau}{2} - \frac{1}{\omega_i} = 0.0099 \text{ s} \tag{26}$$

for $\omega_i = 10000$ rad/sec and $\tau = \frac{1}{f} = 0.02$ s. The proportional gain can be determined by following the procedures of H_∞ control design proposed in [29] and [30] or simply by tuning with trial-and-error.

TABLE 1. System parameters.

Parameters	Values
AC voltage (RMS)	230 V
System fundamental frequency	50 Hz
Switching frequency	10 kHz
Inductor L	2.2 mH
Inductor L_a	2.2 mH
Capacitor C	110 μF
Auxiliary capacitor C_a	165 μF
Voltage V_{DC}	400 V

VI. EXPERIMENTAL VALIDATION

In order to verify the proposed control method, a test rig that consists of a 1.1 kW single-phase PWM-controlled rectifier and three kinds of ripple eliminators was built. The system parameters are summarized in Table 1. In this study, the ripple voltage ratio is selected below 10% for all the auxiliary capacitor voltage references from 500 V to 700 V. According to (6), C_a should be around 160 μF and is chosen as $C_a = 165\,\mu$F. Of course, this ratio could be greater than 10% in order to further decrease the capacitance needed as long as the auxiliary capacitor voltage is higher than the DC-bus voltage to guarantee the successful operation of the eliminator.

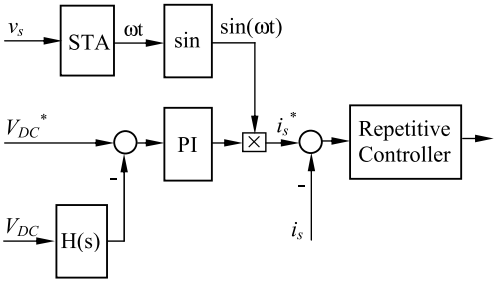

FIGURE 8. Controller for a single-phase PWM-controlled rectifier.

A. CONTROL OF THE SINGLE-PHASE PWM-CONTROLLED RECTIFIER

The PWM rectifier is adopted as an example for generating voltage/current ripples in a DC system. It is controlled to draw a clean sinusoidal current from the source that is in phase with the voltage source. This can be achieved with the controller shown in Figure 8, which mainly consists of three parts: 1) a synchronisation unit to generate a clean sinusoidal current signal that is in phase with the source so that the reactive power drawn from the supply is controlled to be zero; 2) a PI voltage controller that maintains the voltage V_{DC} according to the DC-bus reference voltage V_{DC}^* to generate the right amplitude for the current reference; and 3) a current controller to track the reference current that is formed according to the PI voltage controller and the synchronisation signal. Here, the sinusoid-tracking algorithm (STA) [34] is adopted to provide the phase information

$\sin \omega t$ for the input current, as shown in Figure 8. In order to obtain the DC component of the DC-bus voltage, the hold filter (24) is adopted to remove the voltage ripples. This is able to reduce the ripple component in the reference current, which helps improve the power quality of the current drawn from the voltage source.

Since the reference current is periodic, the repetitive controller designed for the ripple eliminator can also be adopted to track the reference current, as shown in Figure 8.

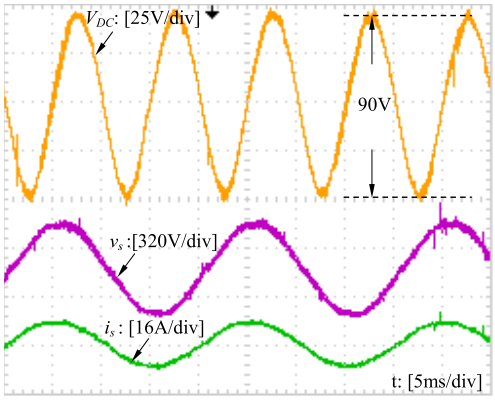

FIGURE 9. Experimental results when the ripple eliminator was not activated: DC-bus voltage V_{DC}, input voltage v_s and input current i_s.

B. VALIDATION

1) WITHOUT THE RIPPLE ELIMINATOR

Figure 9 shows the experimental results of the single-phase PWM-controlled rectifier without the ripple eliminator. The input current was well regulated to be in phase with the source voltage to achieve the unity power factor. However, the ripple of the V_{DC} is around 90 V, which is often not acceptable in practice.

2) WITH THE RIPPLE ELIMINATOR ACTIVATED

Figure 10 shows the results with the ripple eliminator activated. In order to investigate how the voltage V_a affects the reduction of the voltage ripple, different levels of the V_a at 500 V, 600 V and 700 V were tested. Generally, it can be seen that the DC-bus voltage ripple was significantly reduced for all these three voltages. The performance is improved when the auxiliary capacitor voltage is increased because the inductor current tracking performance is improved when the auxiliary capacitor voltage increases. The DC-bus voltage ripple is around 2.5 V when the auxiliary capacitor voltage is 600 V and 700 V, which represents 36 times of improvement. Moreover, the voltage ripple on the auxiliary capacitor decreased with the increase of its DC voltage. The corresponding voltage ripples ΔV_{DC} and ΔV_a are shown in Figure 11. Based on the analysis in Section III, the product of ΔV_a and V_{a0} should be a constant if the auxiliary capacitor is not changed. Indeed, the product is equal to about 25000 for the three different voltages 500 V, 600 V or 700 V. Moreover, the current ripple of the auxiliary inductor shown in Figure 10(b) crosses zero in most of PWM cycles.

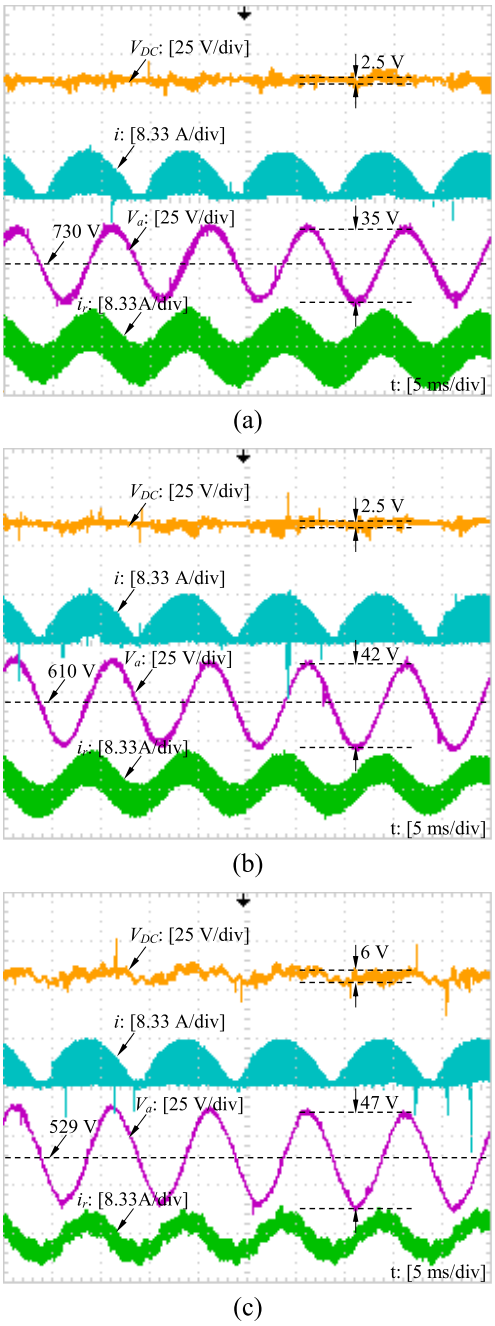

FIGURE 10. Experimental results with different auxiliary capacitor voltages: (a) $V_a^* = 700$ V. (b) $V_a^* = 600$ V. (c) $V_a^* = 500$ V.

The high-frequency current ripples of the auxiliary-inductor current increased along with the increase of the auxiliary-capacitor voltage. Figure 12 shows the theoretical and experimental results of the auxiliary-inductor current ripples Δi_r. It can be seen that the experimental results match the calculated values well.

3) DYNAMIC PERFORMANCE

The dynamic performance of the ripple eliminator was tested. As shown in Figure 13(a), the voltage ripple was almost

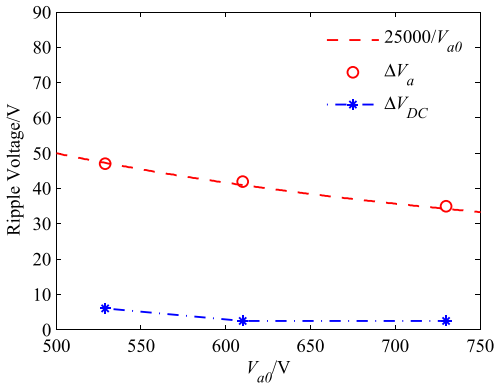

FIGURE 11. Voltage ripples on the DC bus (ΔV_{DC}) and the capacitor C_a (ΔV_a) of the proposed ripple eliminator tested over a wide range of V_{a0}.

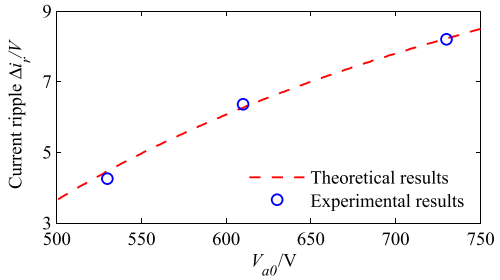

FIGURE 12. Current ripples Δi_r on the inductor L_a over a wide range of V_{a0}.

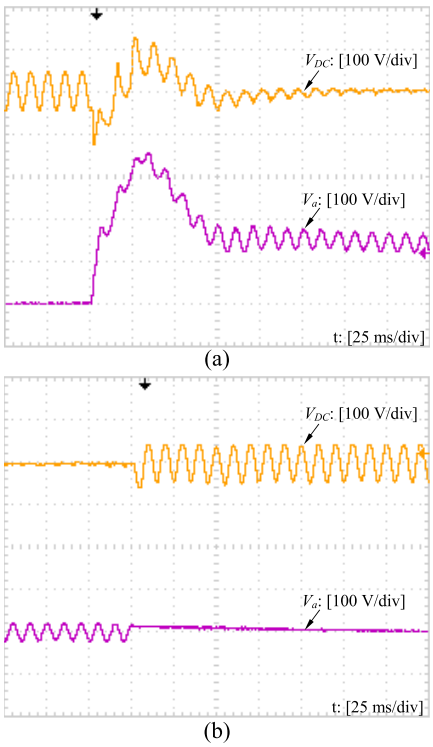

FIGURE 13. Dynamic performance of the proposed ripple eliminator (V^*_{a0} = 600 V): (a) Start-up. (b) Stop.

removed from the DC-bus voltage after the eliminator was activated for about seven line cycles. When the ripple eliminator was deactivated, the ripples of the DC-bus voltage

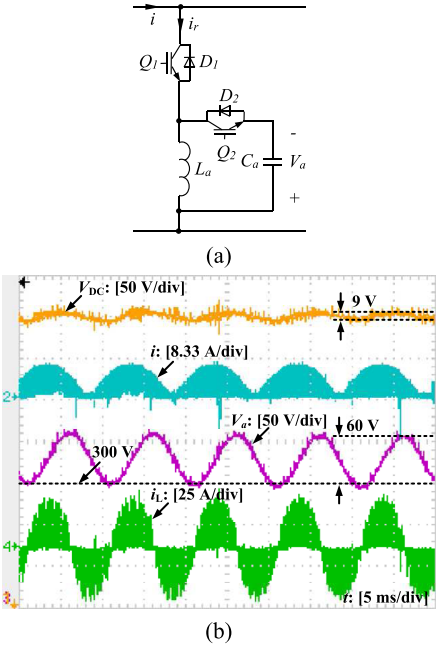

FIGURE 14. The DCM ripple eliminator studied in [19]: (a) topology; (b) experimental results with V^*_{amin} = 300 V.

immediately went back to about 90 V, as shown in Figure 13(b).

4) COMPARISON WITH THE DCM RIPPLE ELIMINATOR IN [19]

The experimental results for the ripple eliminator reported in [19], as shown in Figure 14(a), are presented for comparison. The only difference in this topology is that the power switch Q_2 is swapped with the inductor L_a and the direction of the switch Q_1 is reversed. This makes the ripple eliminator either a buck or a boost converter and hence, both $V_a < V_{DC}$ and $V_a > V_{DC}$ can be achieved.

The inductor L_a is changed to 0.55 mH so that the eliminator can be operated in DCM as studied in [19] and the load is slightly lighter, 1 kW instead of 1.1 kW. The other parameters of the system are the same as given in Table 1. The experimental results are shown in Figure 14(b) when the minimum of the auxiliary voltage was regulated at 300 V. The DC-bus voltage ripple is about 9 V, which is almost 4 times of 2.5 V shown in Figure 10(b) and 10(c) obtained with the proposed control strategy. The investigated eliminator can remove more than 97% of the voltage ripples from the DC bus but the DCM one shown in Figure 14(a) can only eliminate about 90% of the voltage ripples. Moreover, the voltage ripple of the auxiliary capacitor C_a increased to about 60 V because of the lower average voltage. It is also worth noting that the peak value of the compensation ripple current i_r nearly reached 30A, which is about 7 times of the peak current obtained in this paper.

VII. CONCLUSIONS

The concept of ripple eliminators has been further developed to improve the power quality and reduce the voltage ripples

in DC systems and, at the same time, reduce the capacitance needed and the usage of electrolytic capacitors. After deriving the reduction ratio of the capacitance required, the focus of this paper is on the design of an advanced control strategy so that the ripple current can be instantaneously compensated. Compared to [19] and some other related research in the literature, this paper has the following unique contributions: 1) It has been revealed that the capability of of instantly diverting the ripple current away from the DC bus is the key to improve the performance. As a result, ripple eliminators that can be operated in CCM to *instantaneously* divert ripple currents are preferred; 2) the repetitive control strategy is proposed to control one exemplar ripple eliminator, with the ripple energy provided by a single-phase PWM-controlled rectifier. It *instantaneously* compensates the ripple current on the DC bus so that the voltage ripples on the DC bus can be significantly reduced. Experimental results have demonstrated that the proposed strategy is valid and offers several times of performance improvement with comparison to a DCM ripple eliminator reported in [19]. It has been confirmed that it is important to operate ripple eliminators in CCM to instantaneously track the ripple current so that the DC-bus voltage ripples can be minimised to the greatest extent.

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